Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A ferroelectric capacitor, comprising:

a first electrode layer located over a substrate, wherein the first electrode layer includes iridium;

an oxide electrode template located over the first electrode layer;

a ferroelectric dielectric layer located over the oxide electrode template, wherein the oxide electrode template and the ferroelectric dielectric layer have substantially similar crystal structures; and

a second electrode layer located over the ferroelectric dielectric layer.

2. (Original) The ferroelectric capacitor as recited in claim 1 wherein the oxide electrode template forms a portion of a first electrode.

3. (Original) The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template comprises a perovskite material.

4. (Original) The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template comprises a distorted perovskite material.

5. (Original) The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template is selected from the group consisting of $SrIrO_3$ and SrRuO3.

6. (Original) The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template is selected from the group consisting of $BaPbO_3$, $PbIrO_3$, $PbRuO_3$, $BiRuO_3$, $BiIrO_3$, $(La,Sr)CoO_3$, $CaRuO_3$, and $BaPbO_3$.

7. (Original) The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template has a thickness ranging from about 20 nm to about 100 nm.

8. (Original) The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template has a resistivity less than about 400 micro-ohms/cm.

9. (Cancelled)

10. (Original) The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template is a first oxide electrode template and further including a second oxide electrode template located between the ferroelectric dielectric layer and the second electrode layer.

Claims 11-20. (Cancelled)

21. (Currently amended) A ferroelectric random access memory (FeRAM) device, comprising:

a transistor having source/drain regions located over a semiconductor substrate;

an interlevel dielectric layer located over the transistor, the interlevel dielectric layer having a conductive plug therein contacting at least one of the source/drain regions; and

a ferroelectric capacitor located over the interlevel dielectric layer and contacting the conductive plug, including;

a first electrode layer located over the interlevel dielectric layer, wherein the first electrode layer includes iridium;

an oxide electrode template located over the first electrode layer;

a ferroelectric dielectric layer located over the oxide electrode template, wherein the oxide electrode template and the ferroelectric dielectric layer have substantially similar crystal structures; and

a second electrode layer located over the ferroelectric dielectric layer.

22. (Original) The ferroelectric random access memory (FeRAM) device as recited in Claim 21 wherein at least a portion of the transistor includes a nickel silicide.